RISC-V Open and Thriving

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Agenda

- Introduction
- Platforms
- Toolchains
- Language runtimes
- RTOSs
- Bootloaders
- Kernel
- Distributions
Introduction

- `RISK-five`
- Originated at UC Berkeley
- New ISA for education purposes
  - Iterated over 4 years
  - Feedback from building hardware and software
Introduction

• RISC-V Foundation
  – Custodian for ISA specifications
  – 300+ members

• Several chip companies
  – SiFive, Andes, ….
RISC-V Cores and SoC Overview

This document captures the status of various cores and SoCs that endeavor to implement the RISC-V specification. Note that none of these cores/SoCs have passed the in-development RISC-V compliance suite.

Please add to the list and fix inaccuracies.

<table>
<thead>
<tr>
<th>Name</th>
<th>Supplier</th>
<th>Links</th>
<th>Priv. spec</th>
<th>User spec</th>
<th>Primary Language</th>
<th>Licen:</th>
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<tr>
<td>rocket</td>
<td>SiFive, UCB Bar</td>
<td>GitHub</td>
<td>1.11-draft</td>
<td>2.3-draft</td>
<td>Chisel</td>
<td>BSD</td>
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<td>BSD</td>
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<td>Machine (BOOM)</td>
<td>VectorBlox</td>
<td>GitHub</td>
<td>RV32IM</td>
<td>VHDL</td>
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Software Ecosystem - Platforms

• Qemu Emulator
  – Emulate RISC-V on x86
  – Emulate x86 on RISC-V
  – 4.1 Release
    • Spike Machine Model
    • ISA 1.11 support
    • CPU topologies in device tree

• HiFive Unleashed
  – FU500 Base Platform
config.sub patch for RISC-V

From: Palmer Dabbelt
Subject: config.sub patch for RISC-V
Date: Wed, 10 Sep 2014 19:20:31 -0700

This patch provides support for the RISC-V ISA: [http://riscv.org/](http://riscv.org/)

Not yet upstreamed ports of the binutils, GCC, LLVM, glibc, and Linux exist for RISC-V, and a number of hardware implementations exist -- more more information can be seen at [http://riscv.org](http://riscv.org). We'd like to start getting RISC-V recognized by configure so it's easier for people to start porting stuff.

Thanks!
Software Ecosystem - Toolchains

• GCC based toolchains
  – Upstream since 7.1
  – Glibc
    • RV64 Upstream since 2.27
  – Newlib
    • 2.50+

• LLVM/Clang
  –CodeGen for RV32/RV64
  – Experimental in 8.0 release
  – Promoted to mainstream backend in upcoming 9.0 release
  – Unleashed rust ecosystem
Software Ecosystem - Toolchains

• Musl C library port is now upstream
  – Tested on rv64
  – Musl is system C library for Alpine, OpenWRT
Software Ecosystem - debuggers

- GDB support upstream
  - 8.2 Bare-metal support
  - Upcoming in 8.3 Hosted OS apps (Linux, BSD)
  - No gdbserver
- LLDB support in process
- Debug and trace kits
  - SweRV, J-Link,
- OpenOCD
  - FTDI, USB probes
- Commercial solutions
  - Lauterbach, IARM, SEGGER
Software Ecosystem - Languages

- **Golang**
  - Can run docker
    - [https://github.com/carlosedp/riscv-bringup](https://github.com/carlosedp/riscv-bringup)
  - No CGO
  - Not Upstream yet

- **Rust on RISC-V**
  - [https://github.com/rust-embedded/riscv](https://github.com/rust-embedded/riscv)
  - [https://github.com/rust-embedded/riscv-rt](https://github.com/rust-embedded/riscv-rt)
Operating Systems - RTOS

- [https://github.com/riscv/riscv-software-list#real-time-operating-systems](https://github.com/riscv/riscv-software-list#real-time-operating-systems)
  - Zephyr
    - HiFive1
  - FreeRTOS
    - Upstream support in 10.2+
  - QEMU
    - Runs RTOSes
Bootloaders

- BBL (Berkeley Boot Loader)
- OpenSBI
  - New implementation
  - Spec - https://github.com/riscv/riscv-sbi-doc
- U-Boot
- Coreboot
Linux Kernel

• Upstream Since 2018
  – QEMU, HiFive Unleashed
  – BPF JIT
  – NOMMU
  – 5.3 Release has, Huge Pages, highres timers, dynamic ticks
  – 80 RISCV arch port contributors and growing
Get Involved

- [sw-dev@groups.riscv.org](mailto:sw-dev@groups.riscv.org)
- [#riscv on Freenode](https://freenode.net)
- Respective Project’s upstream mailing lists
  - Kernel
    - [linux-riscv@lists.infraread.org](mailto:linux-riscv@lists.infraread.org)
Linux Distributions

- Fedora
  - [https://fedoraproject.org/wiki/Architectures/RISC-V](https://fedoraproject.org/wiki/Architectures/RISC-V)
- Debian
- OpenSuSE
  - [https://en.opensuse.org/openSUSE:RISC-V](https://en.opensuse.org/openSUSE:RISC-V)
- Gentoo
- Yocto
  - [https://github.com/riscv/meta-riscv](https://github.com/riscv/meta-riscv)
- Buildroot - Upstream
- OpenWRT
  - [https://openwrt.org/docs/techref/hardware/soc/soc.sifive](https://openwrt.org/docs/techref/hardware/soc/soc.sifive)
Thank you