

Open source ecosystem POWERing innovation in FPGA and ASIC development

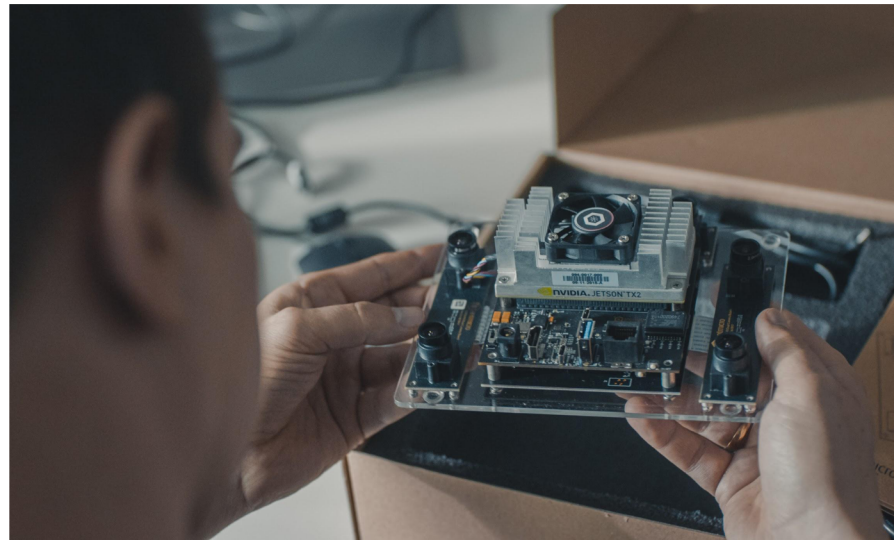
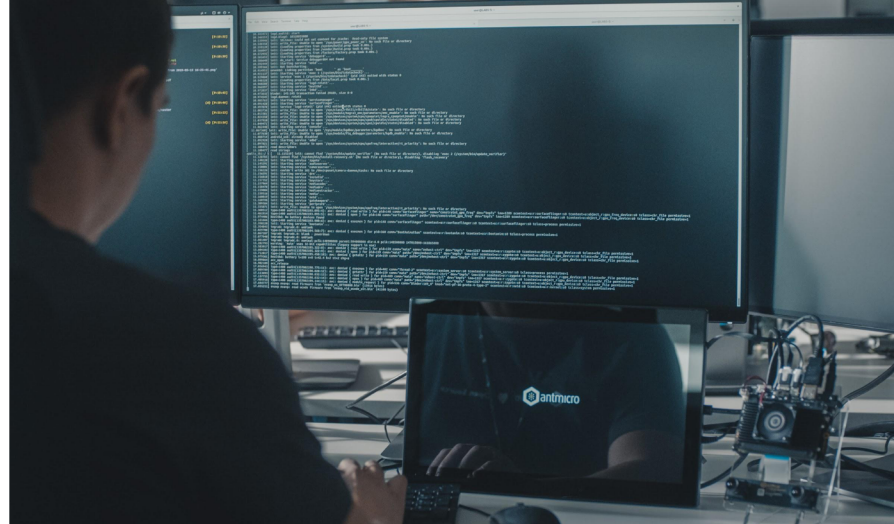
OpenPOWER Summit NA, 2020-09-15

Michael Gielda, mgielda@antmicro.com



ANTMICRO & OPEN SOURCE

- Founded in 2009, open source is key to our business model
- We provide open source services to transform industries by building **new workflows and design methodologies** based on open source
- Also use them ourselves to build software-driven products for our customers



WHAT WE DO



HARDWARE

Proof of Concepts (PoC),
demonstrators, prototyping,
open source platforms



SOFTWARE & AI

OS porting, building BSPs,
build systems, device
management, edge & cloud
AI



FPGA & ASIC

Custom IP blocks, SiP
development, soft SoCs,
heterogeneous processing
systems



TOOLS

Tools, new software and
hardware development and
testing methodologies

WHAT WE DO

- To learn more about us, just see our tech showcase on the main page

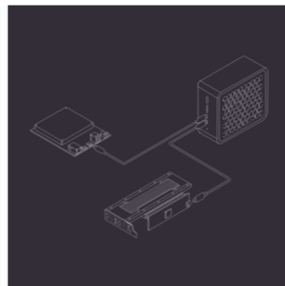
TECHNOLOGY SHOWCASE:



Linux GUIs on Zynq with FastVDMA, HDMI and Snickerdoodle



seL4 on RISC-V in Renode



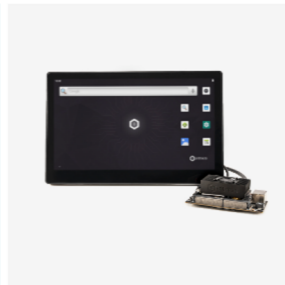
Plug-and-play AI acceleration with Thunderbolt



Antmicro's open source SDI-to-MIPI Bridge



Renode 1.10 release



Android on open Jetson Nano / Xavier NX baseboard



ORGANIZATIONS WE TAKE PART IN

- We typically play a strategic / connecting / early adopter and ecosystem role
- We believe especially in collaborations across the hardware / software domains, between industries and interest groups with common goals
- Open source = may the best one win (or rather, a connected network of best ones)
- “Open source lifts all boats” - organizations that create real open source collaterals can be seen extensions of one another, as the “IP” can be reused, repurposed, combined, rehashed

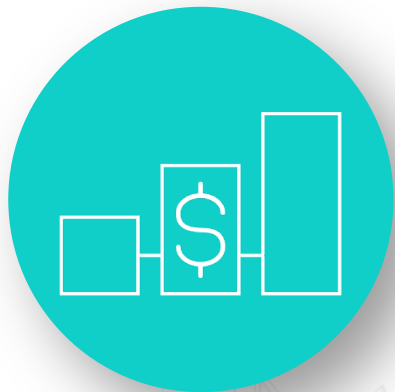


WHY ANTMICRO JOINED OPENPOWER

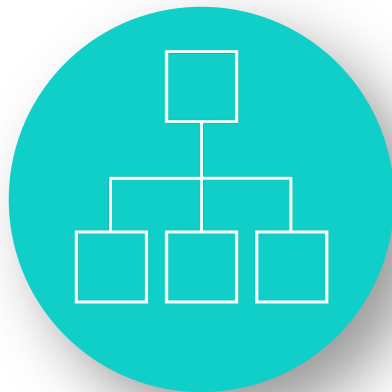
- Open sourcing of POWER ISA put it back on our and our customer's radar, great enthusiasm built around Microwatt
- Cloud and datacenter increasingly in our focus
- Edge increasingly back in OpenPOWER's focus
- [Joined in May 2020](#)
- Added support for POWER in Renode, with Microwatt as first target
- Connecting POWER to open source ASIC/FPGA ecosystem, commercial open source services



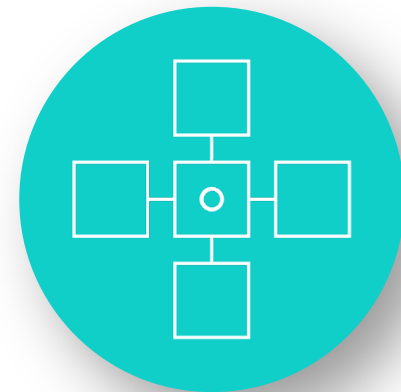
COMPUTE AND DESIGN CHALLENGES



Costs of hardware
increasing
significantly

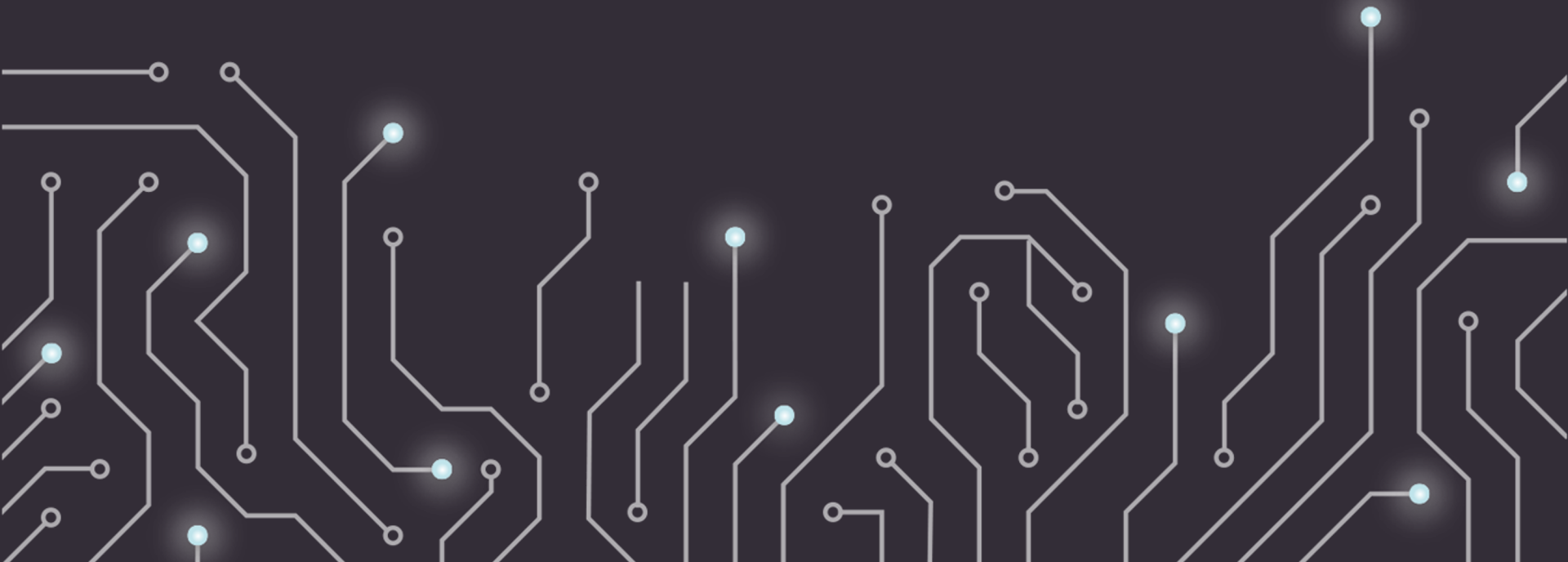


Innovation often stalled
in corporate structures



Need more
purpose built
architectures

ASIC AND FPGA: A LONG BUT HOPEFUL JOURNEY TOWARDS OPEN SOURCE



OPEN SOURCE PDK

- Collaboration: Google, SkyWater, efabless, Blue Cheetah, Antmicro and academic partners, CHIPS Alliance
- SkyWater technology foundry accredited by the US Department of Defense
- A historical first open source, manufacturable [SkyWater PDK](#) (Process Design Kit) for the 130 nm MOSFET fabrication process
- Open source PDK release accompanies by **free shuttle run for open source designs**
- SKY130 process node will be followed by other, more advanced nodes (90 and 45 nm - A2I territory)



CONTRIBUTE TO SKYWATER-PDK

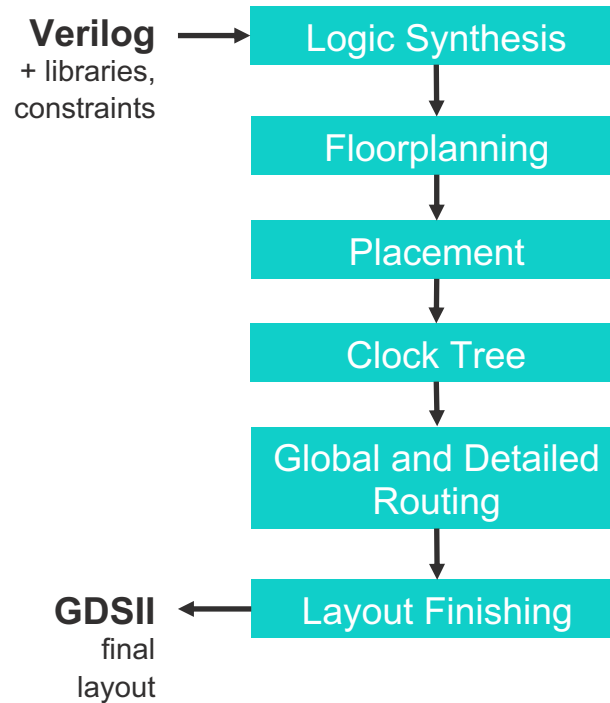
- T-shirt giveaway for [project](#) contributors and fans
 - building a community in more ways than code!
- Made by Antmicro & Google
- Contribution [guidelines](#)
- Lots of help needed!
- See the [incredibly popular talk by Tim Ansell](#) (Google) from FOSSi Dial-Up



OPEN ROAD: 24H, NO HUMANS IN LOOP, OPEN SOURCE EDA

- DARPA [Idea Program](#)
- Part of CHIPS Alliance (see talk on Thursday)
- Open source, fully automated digital design flow
- “Linux of EDA”, reduce cost & risk
- No human-in-the-loop (NHIL) design, replaced by machine learning, 24-hour turnaround
- Bring research closer to industry and designers
 - Enable critical algorithm innovation by providing functional framework
- Initial goal - RTL-to-GDSII phase of SoC design
- More information at <https://github.com/The-OpenROAD-Project>

OpenROAD



VERIBLE

- <https://github.com/google/verible>
- flex/yacc SV 2017 parser
- used at Google - OpenTitan, RISC-V-DV, other projects
- integrated with FuseSoC for linting and formatting SV code - [read our blog note](#)

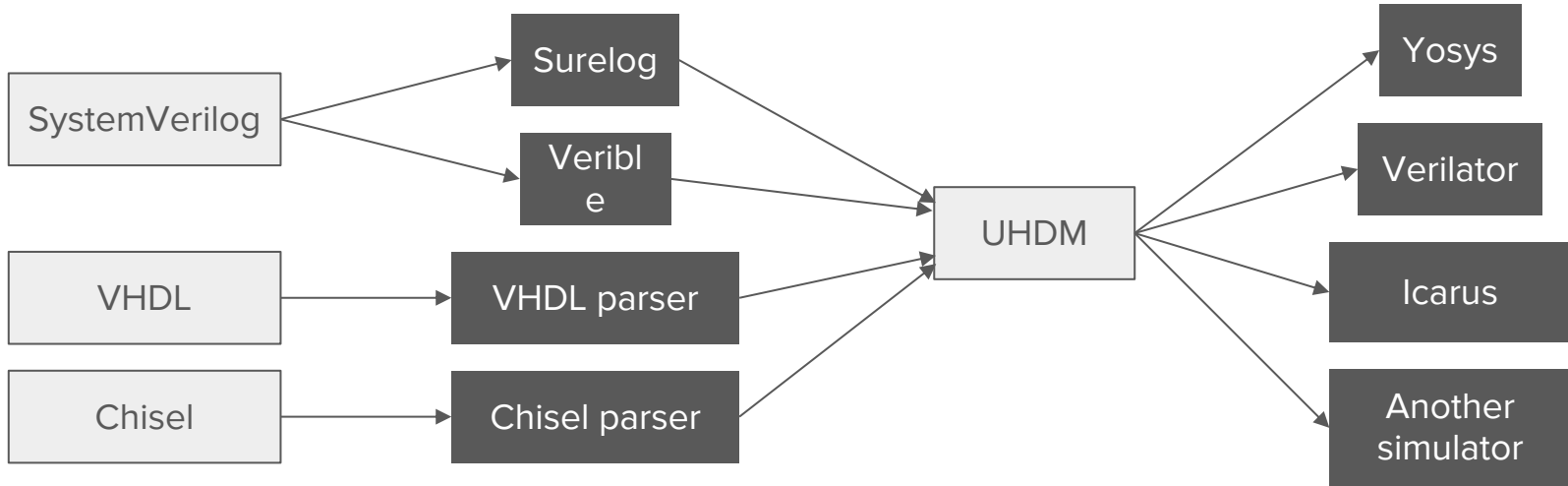


SURELOG / UHDM

- <https://github.com/alainmarcel/Surelog>
- System Verilog 2017 pre-processor, parser, UHDM compiler
- IEEE Design/TB VPI and Python AST API
- UHDM - interop library for connecting front- and back-end of various tools in a modular fashion
- developed in collaboration between Google and Antmicro into a pluggable SV front-end for various open source tools



UHDM - SV FRONTEND AND INTEROP LIBRARY (TARGET)



EXTENDING VERILATOR

- Simulates the RTL with high performance by compiling to an optimized model and wrapping inside a C++/SystemC/C++-under-Python module
- Outperforms many proprietary alternatives
- Developing fast, with work from author (Wilson Snyder), FOSSi community and - of course - CHIPS Alliance, led by Antmicro - adding support for SystemVerilog / UVM
- <https://github.com/verilator/verilator>



		icarus	moore	moore_parse	odin	slang	surelog	sv2v_zachjs	sv_parser	tree_sitter_verilog	verible	verilator	yosys
Ariane RISC-V core	ariane	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1/1	0/1	0/1	0/1	0/1
Tests imported from Basejump STL	basejump	0/302	32/302	164/302	0/302	97/302	289/302	292/302	296/302	0/302	299/302	98/302	0/302
BlackParrot RISC-V core	black-parrot	0/4	0/4	0/4	0/4	0/4	0/4	0/4	4/4	0/4	0/4	0/4	0/4
	earlgrey	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
FX68K m68k core	fx68k	0/1	0/1	1/1	0/1	1/1	1/1	1/1	1/1	0/1	1/1	1/1	0/1
Tests imported from hdlConvertor	hdlconv	0/306	78/306	127/306	8/306	69/306	283/306	87/306	305/306	191/306	261/306	67/306	44/306
Ibex RISC-V core	ibex	0/1	0/1	0/1	0/1	0/1	1/1	1/1	1/1	0/1	1/1	1/1	0/1
Tests imported from ivtest	ivtest	0/2173	451/1902	1474/1902	298/1902	1354/1902	1868/2173	1484/1902	1899/1902	34/1902	1873/1902	1501/2173	450/2173
RSD RISC-V core	rsd	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1/1	0/1	0/1	0/1	0/1
Various sanity checks	sanity	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
SCR1 RISC-V core	scr1	0/1	0/1	0/1	0/1	0/1	1/1	1/1	1/1	0/1	0/1	0/1	0/1
SwERV RISC-V core	swerv	0/1	0/1	0/1	0/1	0/1	1/1	1/1	0/1	0/1	0/1	1/1	0/1
Taiga RISC-V core	taiga	0/1	0/1	0/1	0/1	0/1	1/1	0/1	1/1	0/1	1/1	0/1	0/1
Tests imported from utd-SystemVerilog	utd-sv	0/295	114/295	292/295	103/295	119/295	294/295	287/295	260/295	272/295	294/295	125/295	286/295
Tests imported from UVM	uvm	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1/1	1/1	1/1	0/1	0/1
Tests imported from Yosys	yosys	9/184	132/184	155/184	72/184	167/184	184/184	172/184	183/184	164/184	176/184	169/184	154/184
White space	5.3	6/7	7/7	7/7	1/7	7/7	7/7	7/7	7/7	0/1	1/1	7/7	7/7
Comments	5.4	6/7	7/7	7/7	0/7	7/7	7/7	7/7	7/7	1/1	1/1	7/7	7/7
Identifiers, keywords, and system names	5.6	1/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2
Escaped identifiers	5.6.1	0/2	2/2	2/2	1/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2

```

Surelog
description: Full swerv core test
rc: 0 (means success: 1)
should_fail: 0
tags: swerv
incdirs: /tmpfs/src/github/sv-tests/third_party/cores/swerv/design/include /tmpfs/src/github/sv-tests/third_party/cores/swerv/design/include
top_module: swerv_wrapper
type: parsing
mode: parsing
files: third_party/cores/swerv/configs/snapshots/default/common_defines.vh third_party/cores/swerv/design/include/b
time elapsed: 71.444s
swerv

```

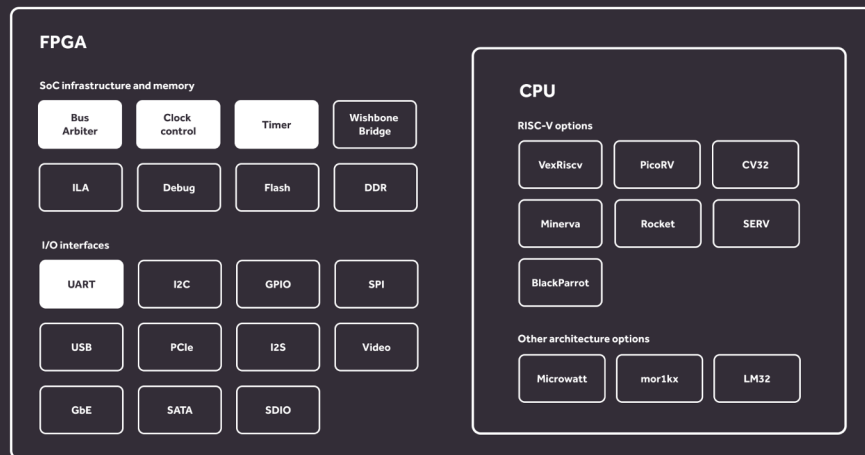
```

third_party/cores/swerv/configs/snapshots/default/common_defines.vh
1 // NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE NOTE
2 // This is an automatically generated file by joseph.rahme on Tue Oct 15 13:13:16 PDT 2019
3 //
4 // cmd: swerv -snapshot=default -ahb_lite
5 //
6 `define RV_INST_ACCESS_MASK5 'hfffffff
7 `define RV_DATA_ACCESS_ENABLE4 1'h0
8 `define RV_INST_ACCESS_ENABLE3 1'h0
9 `define RV_INST_ACCESS_ENABLE0 1'h0
10 `define RV_INST_ACCESS_MASK3 'hfffffff
11 `define RV_DATA_ACCESS_ENABLE5 1'h0
12 `define RV_DATA_ACCESS_MASK5 'hfffffff

```

LITEX

- SoC builder / IP library for SoCs
- Portable between various FPGAs
- Delivers a set of IP blocks - DRAM, Ethernet, USB, PCIe, SATA, SD...
- Support for Microwatt
- Well supported in a robust software ecosystem - Zephyr, Linux, Renode, Verilator, SymbiFlow
- Actively developed by Florent Kermarrec in collaboration with Antmicro and a wide array of users
- <https://github.com/enjoy-digital/litex>



OPEN SOURCE DRAM CONTROLLER

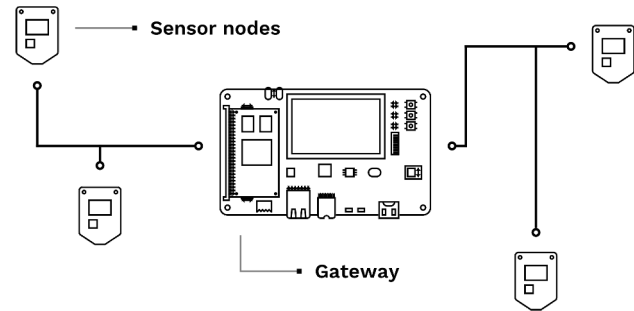
- best-in-class open source DDR3/4 DRAM controller for FPGA
- cross-platform, portable, modular and well-tested, developed in collaboration between Antmicro and creator, Florent Kermarrec
- currently work on ASIC-proofing
- used as experimentation platform for research
- <https://github.com/enjoy-digital/litedram>

LITEDRAM

RENODE

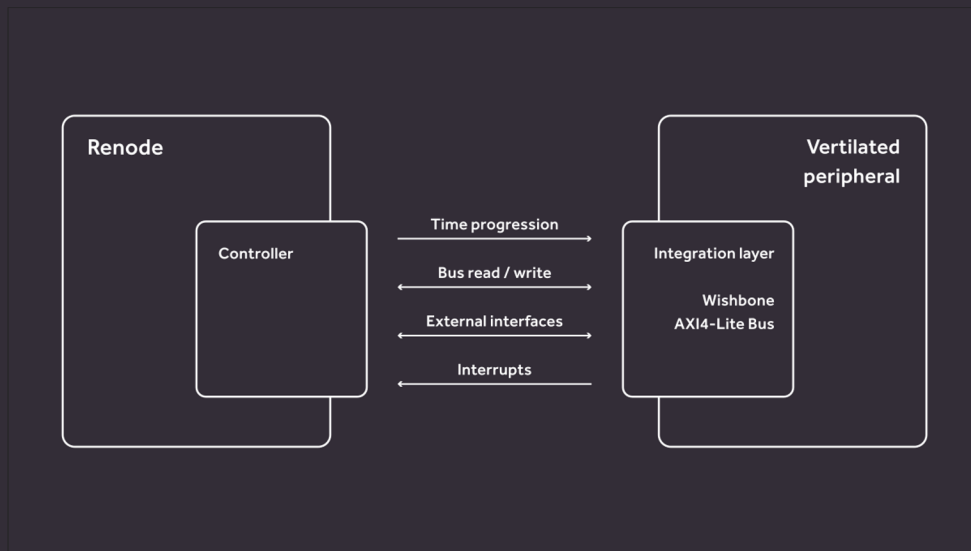
- Open source, highly configurable simulation framework from Antmicro - <https://renode.io/>
- Rapidly create and develop software for complex setups without changing/recompiling the simulator
- Execute, debug and test embedded software with a rich feature set and many integrations
- Supports various IP, sensor, network building blocks so you can quickly build and simulate entire SoCs/systems
- Used for OS porting, CI testing, ML framework testing/benchmarking, HW/SW co-development and many other purposes

RENODE™



RENODE FOR HW PROTOTYPING AND DEVELOPMENT

- Ability to co-simulate with Verilator or physical hardware
- Configuration over recompilation, lots of extensibility (Python, plugins)
- Customers have found it easier to build Renode models than HDL, could get new iterations of working software in days rather than weeks
- Ability to do custom instructions via plugins, execution hooks, fine grained control etc.
- Supports LiteX and OpenPOWER!



```

antmicro@renode-dell: ~/renode-hq-master/renode
File Edit View Search Terminal Help
21
20 Execute Command sysbus.gpioInputs.user_switch_1 Toggle
19 Test If Uart Is Idle 5
18
17 Should Generate Interrupts On Gpio Both Edges
16 Create Machine riscv-interrupt-blinky-gpio_interrupts-edge_both.elf-s_134928-d90257bf
15 Create Terminal Tester ${UART}
14
13 Start Emulation
12
11 Wait For Line On Uart CoreTIMER and external Interrupt Example.
10 Wait For Line On Uart Observe the LEDs blinking on the board. The LED patterns changes every
9
8 Test If Uart Is Idle 5
7
6 Execute Command sysbus.gpioInputs.user_switch_0 Toggle
5 Wait For Line On Uart GPIO1
4
3 Execute Command sysbus.gpioInputs.user_switch_0 Toggle
2 Wait For Line On Uart GPIO1
1
157 Execute Command sysbus.gpioInputs.user_switch_1 Toggle
MiV.robot 157,17 62%

```

```

antmicro@renode-dell: ~/renode-hq-master/renode
File Edit View Search Terminal Help
antmicro@renode-dell:~/renode-hq-master/renode$ ./test.sh tests/platforms/MiV/MiV.robot
Preparing suites
Starting suites
Running tests/platforms/MiV/MiV.robot
=====
MiV
=====
Should Blink Led Using Systick | PASS |
-----
Should Blink Led Using CoreTimer | PASS |
-----
Should Run FreeRTOS Sample | PASS |
-----
Should Run LiteOS Port Sample | PASS |
-----
Should Generate Interrupts On Gpio Rising Edge | PASS |
-----
Should Generate Interrupts On Gpio Falling Edge | PASS |
-----
Should Generate Interrupts On Gpio Both Edges | PASS |
-----
Should Generate Interrupts On Gpio High Level | PASS |
-----
Should Generate Interrupts On Gpio Low Level | PASS |
-----
MiV | PASS |
-----
9 critical tests, 9 passed, 0 failed

```

TEST SUITE TEST LOG

20190729 13:31:14 GMT+02:00 | 1 day 5 hours ago

Log level:

Test Statistics

Total Statistics	Total	Pass	Fail	Elapsed	Pass / Fail
Critical Tests	6	6	0	00:02:39	<div style="width: 100%; height: 10px; background-color: green;"></div>
All Tests	6	6	0	00:02:39	<div style="width: 100%; height: 10px; background-color: green;"></div>
Statistics by Tag					
No Tags					<div style="width: 100%; height: 10px; background-color: #ccc;"></div>
Statistics by Suite					
Test Suite	6	6	0	00:02:42	<div style="width: 100%; height: 10px; background-color: green;"></div>

Test Execution Log

SUITE Test Suite	00:02:42.304
Full Name: Test Suite	
HotSpot Action: -	
Source: /tmp/45-pipeline/SAME70.robot	
Start / End / Elapsed: 20190729 13:28:32.325 / 20190729 13:31:14.629 / 00:02:42.304	
Status: 6 critical test, 6 passed, 0 failed 6 test total, 6 passed, 0 failed	
SETUP renode-keywords.Setup	00:00:03.419
TEARDOWN renode-keywords.TearDown	00:00:00.003
TEST Single Node Should Send A PDelay Request Packet	00:00:05.597
TEST Slave Should Call The Phase Dis Callback	00:00:18.705
TEST Master Should Send Announce Packets With The Expected Parameters	00:00:07.651
Full Name: Test Suite.Master Should Send Announce Packets With The Expected Parameters	
Start / End / Elapsed: 20190729 13:29:00.115 / 20190729 13:29:07.766 / 00:00:07.651	

LINUX-LITEX-VEXRISCV-PIPELINE

A Linux build running on the LiteX soft SoC



[CONTAINER](#)
[FULL HISTORY](#) →

Last launch: Pass

07/13/2019, 10:24 | e5314db | 00:01:49

[DETAILS](#) →

RIOT-CC2538DK-PIPELINE



[CONTAINER](#)
[FULL HISTORY](#) →

Last launch: Pass

07/13/2019, 10:42 | cea907d | 00:00:32

[DETAILS](#) →

RPL UDP IN CONTIKI-NG ON CC2538DK

Two **CC2538** nodes running Contiki-NG connected with RPL-UDP



[CONTAINER](#)
[FULL HISTORY](#) →

Last launch: Pass

07/13/2019, 10:24 | 7f6d340 | 00:05:34

[DETAILS](#) →

ZEPHYR TSN/GTPP ON SAM E70



[CONTAINER](#)
[FULL HISTORY](#) →

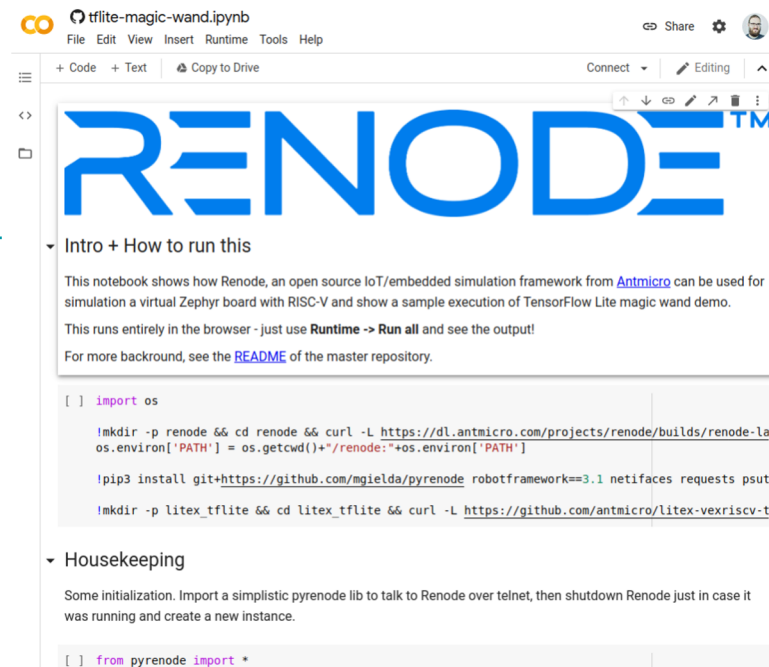
Last launch: Pass

07/04/2019, 11:03 | 9ecc6cd | 00:10:06

[DETAILS](#) →

RENODE

- You can try it out without installation/setup (or even without knowing how it works)
- <https://colab.research.google.com/github/mgielda/renode-notebooks-ipynb/blob/master/tflite-magic-wand.ipynb>



The screenshot shows a Jupyter Notebook interface with the following content:

RENODE™

Intro + How to run this

This notebook shows how Renode, an open source IoT/embedded simulation framework from [Antmicro](#) can be used for simulation a virtual Zephyr board with RISC-V and show a sample execution of TensorFlow Lite magic wand demo.

This runs entirely in the browser - just use **Runtime -> Run all** and see the output!

For more background, see the [README](#) of the master repository.

```
[ ] import os

mkdir -p renode && cd renode && curl -L https://dl.antmicro.com/projects/renode/builds/renode-la
os.environ['PATH'] = os.getcwd()+"/renode:"+os.environ['PATH']

pip3 install git+https://github.com/mgielda/pyrenode robotframework==3.1 nifaces requests psut

mkdir -p litex_tflite && cd litex_tflite && curl -L https://github.com/antmicro/litex-vexriscv-t
```

Housekeeping

Some initialization. Import a simplistic pyrenode lib to talk to Renode over telnet, then shutdown Renode just in case it was running and create a new instance.

```
[ ] from pyrenode import *
```

SYMBIFLOW

- Fully open source toolchain for FPGA development
- Aims to provide an end-to-end FPGA flow
- Multiple vendors
- Collaboration with QuickLogic - first vendor-supported open source FPGA toolchain, developed by Antmicro
- Makes FPGA development software-centric and collaborative
- **Vital for research, prototyping**, niche uses - already good results for specific scenarios
- With open tools, FPGAs can be “mundane” part of future SoCs
- <https://symbiflow.github.io/>

The logo for SymbiFlow, with the text "SymbiFlow" in a bold, purple, sans-serif font.The logo for QuickLogic, featuring the text "QuickLogic" in a bold, black, sans-serif font, with a stylized graphic of three curved lines (red, grey, and red) to the left.

Supported Architectures

Xilinx 7-Series

The most popular Xilinx
FPGA family

[learn more](#)

Lattice ice40

World's smallest FPGAs
for mobile devices

[learn more](#)

Lattice ecp5

Low cost FPGAs with
high performance features

[learn more](#)

QuickLogic EOS S3

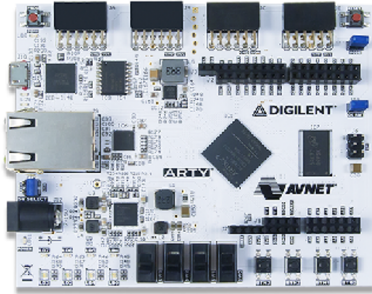
FPGA + CPU
sensor processing platform

[learn more](#)

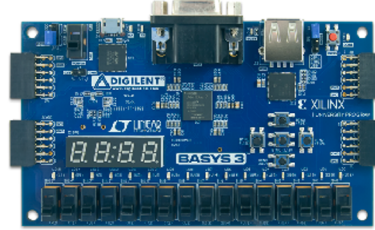
Do you want to add more?

Help us!

[learn more](#)



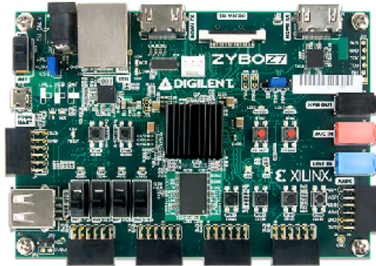
Digilent Arty A7-35T
XC7A35T



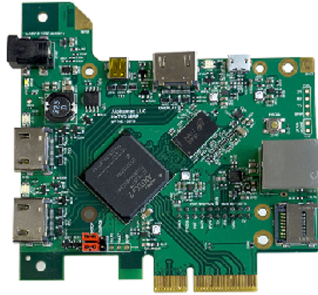
Digilent Basys 3 Artix-7
XC7A35T



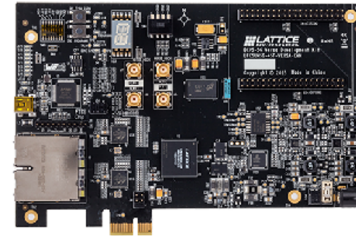
QuickFeather Development Kit
EOS-S3



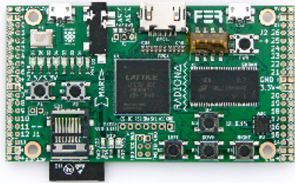
Digilent Zybo Z7
XC7Z010



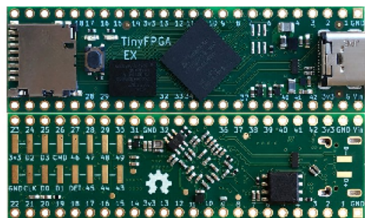
Alphamax NeTV2
XC7A35T



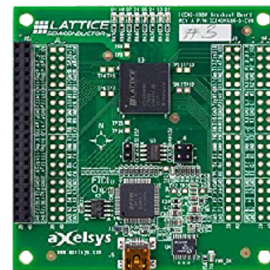
ECP5-5G Versa
LFE5UM5G-45F



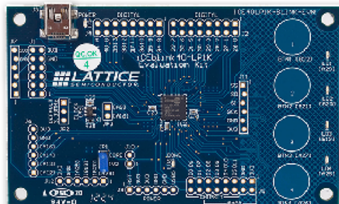
ULX3S
LFE5U-12F-25F-45F-85F



TinyFPGA Ex
LFE5U-85F/LFE5UM5G-85F



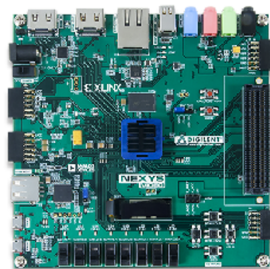
iCE40-HX8K Breakout Board
ICE40HX8K-B-EVN



iCEblink40LP1K Evaluation Kit
ICE40LP1K-BLINK-EVN



iCEstick Evaluation Kit
ICE40HX1K-STICK-EVN



Digilent Nexys Video Artix-7 FPGA
XC7A200T-1SBG484C

SYMBIFLOW CAN NOW ALSO DO VHDL

- via ghdl-yosys-plugin
- see:
<https://ghdl.readthedocs.io/en/latest/using/Synthesis.html>

SymbiFlow

GHDL

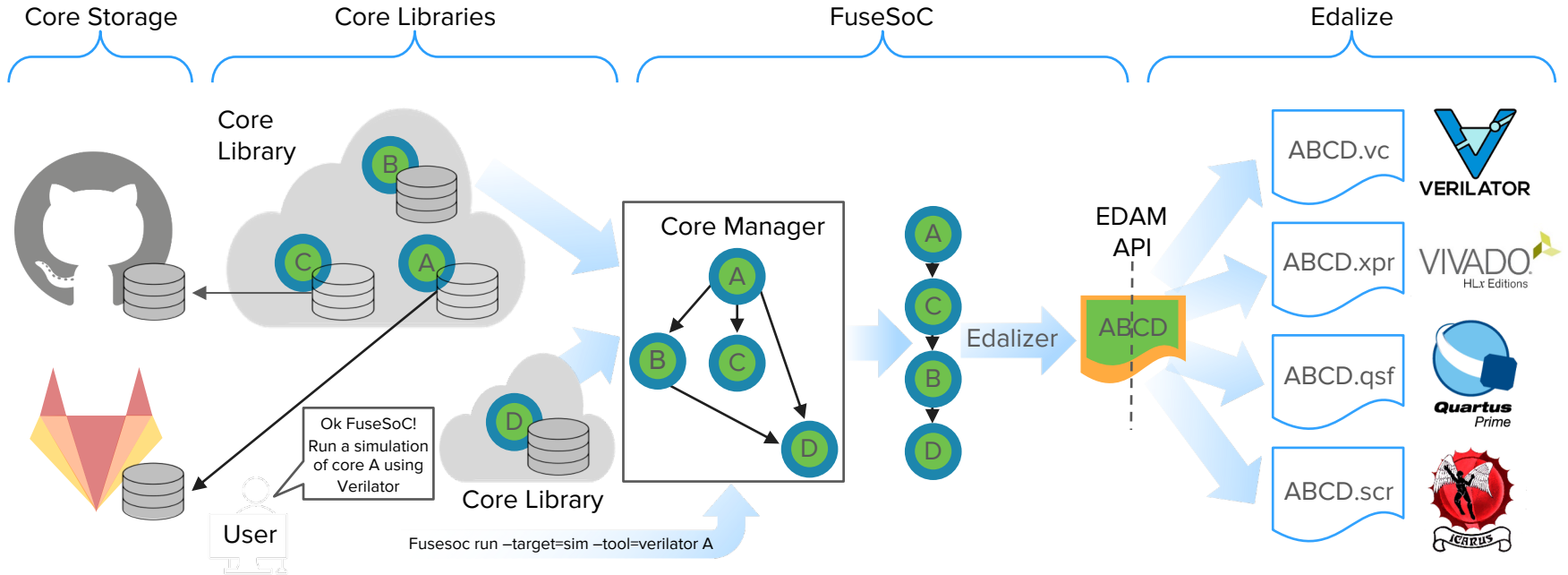
FUSESOC + EDALIZE

- Python package manager and a set of build tools for HDL code to increase IP cores reuse
- Helps creating, building, simulating SoC designs
- Simplifies:
 - reusing existing cores
 - creating compile-time or run-time configurations
 - porting designs to new targets
 - letting other projects use your code
 - setting up CI
- Actively developed by Olof Kindgren, with many contributions from Antmicro, in wide use in the ecosystem - <https://github.com/olofk/fusesoc>



EDALIZE

FUSESOC + EDALIZE



FPGA PERF TOOL

- Tool by Antmicro to analyzes various FPGA EDA tools for Synthesis and Place & Route (both open source and vendor-locked)
- Measures tool performance (MHz, resources, runtime, etc), runtime and quality of results
- Tells you how well your design is faring
- Makes use of [Edalize](#)
- Part of [SymbiFlow](#)
- Available at <https://github.com/SymbiFlow/fpga-tool-perf>



SUMMARY



OUTLOOK: SUNNY, BUT BRING A DEVELOPER ALONG JUST IN CASE

- Really good progress being made towards more collaborative ecosystem for ASIC/FPGA design
- Still, there is a lot of legacy to be untangled here
- But we have managed to reach as far as the PDK, so the sky(water?) is the limit now
- POWER could play a vital role in this ecosystem, aligning with the efforts and benefitting from the rapid development and collaborative effort
- That's what Antmicro wants to enable!



CHIPS ALLIANCE WORKSHOP

- 17 September 2020 - this Thursday!
- **“Enabling Fully Open Source and Continuous Integration-Driven Flows in ASIC and FPGA Development”** - talk about tools WG progress from Antmicro
- Lots of awesome speakers including fellow OpenPOWER Foundation members - UC Berkeley, Google etc.; OpenROAD, SymbiFlow, and other topics
- Check out the [schedule!](#)





THANK YOU
FOR YOUR ATTENTION!

